# SEMICONDUCTOR DEVICE AND TESTING METHOD

## Abstract of the Disclosure

A semiconductor device and a method of testing the semiconductor device are provided. The semiconductor device includes a memory cell array, a sense amplifier, a control circuit, a row decoder, a bitline-pair voltage setting circuit, and a wordline driver. The memory cell array is connected to one of a plurality of wordlines and a plurality of bitline pairs. The memory cell array comprises a plurality of memory cells, wherein each memory cell is connected to one of the plurality of wordlines and the plurality of bitline pairs. The sense amplifier amplifies data read from the memory cell array. The control circuit controls writing/reading of data to/from the memory cell array. The row decoder decodes an address signal and outputs a decoded signal to select one of the plurality of wordlines. The bitline-pair voltage setting circuit sets the voltage of at least one of the plurality of bitline pairs to a bitline test voltage in a test mode. The wordline driver sets the low-level voltages of the plurality of wordlines to a wordline test voltage in the test mode. The wordline test voltage level can be set to be different from the low-level voltage of the plurality of wordlines in a normal operation mode.